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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/605,449 | 09/30/2003 | Dennis R. Conti | BUR920030050US1 | 2448 |

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| EXAMINER | |
|---|---|
| HOLLINGTON, JERMELE M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2829 | |

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/605,449 | CONTI ET AL. | |
| | Examiner | Art Unit | |
| | Jermele M. Hollington | 2829 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2,3,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Allowable Subject Matter*

1. The indicated allowability of claims 2-3 and 8-9 is withdrawn in view of the newly discovered reference(s) to Iino et al (5568054). Rejections based on the newly cited reference(s) follow.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 2-3 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gamache et al (6577146) in view of Iino et al (5568054).

Regarding claim 2, Gamache et al disclose [see Figs. 1-2] a method of controlling the burning in of at least one I/C chip (IC chip 12) in a burn in tool (test fixture 8), wherein said tool (8) has a device (socket 22) for mounting each chip (12) to be burned in, and a power source (power

source 22) to supply electrical current to burn in each chip (12), comprising the steps of: continuously monitoring [via computer 48] at least one electrical value input to each chip (12) selected from the group of current, voltage and power, and varying the voltage [via combination of computer 48, power sensor 46 and power source 44] to maintain at least one of the values at or below a given value. However, Gamache et al do not disclose maintain the current value at or below a given value. Iino et al disclose [see Fig. 6] controlling the burning in of at least one I/C chip (IC chip on wafer W) in a burn in tool (inspection section 12), wherein said tool (12) has a device (probe card 20) for mounting each chip (IC on wafer W) to be burned in, and a power source (power source 40) to supply electrical current to burn in each chip (IC on wafer W), comprising the steps of: continuously monitoring [via measuring section 41] at least one electrical value input to each chip (on wafer W) wherein the current value is maintain at or below a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13]. Further, Iino t al teach that the addition of maintaining current value at or below given value is advantageous because it prevents over current as well as to detect defects of the IC in a wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Gamache et al by adding a measuring section as taught by Iino in order to prevent over current as well as to detect defects of the IC in a wafer.

Regarding claim 3, Gamache et al disclose [see Figs. 1-2] a method of controlling the burning in of at least one I/C chip (IC chip 12) in a burn in tool (test fixture 8), wherein said tool (8) has a device (socket 22) for mounting each chip (12) to be burned in, and a power source (power source 22) to supply electrical current to burn in each chip (12), comprising the steps of: continuously monitoring [via computer 48] at least one electrical value input to each chip (12)

selected from the group of current, voltage and power, and varying the voltage [via combination of computer 48, power sensor 46 and power source 44] to maintain at least one of the values at or below a given value. However, Gamache et al do not disclose maintain the power value at or below a given value. Iino et al disclose [see Fig. 6] controlling the burning in of at least one I/C chip (IC chip on wafer W) in a burn in tool (inspection section 12), wherein said tool (12) has a device (probe card 20) for mounting each chip (IC on wafer W) to be burned in, and a power source (power source 40) to supply electrical current to burn in each chip (IC on wafer W), comprising the steps of: continuously monitoring [via measuring section 41] at least one electrical value input to each chip (on wafer W) wherein the power value is maintain at or below a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13]. Further, Iino t al teach that the addition of maintaining current value at or below given value is advantageous because it prevents over current as well as to detect defects of the IC in a wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Gamache et al by adding a measuring section as taught by Iino in order to prevent over current as well as to detect defects of the IC in a wafer.

Regarding claim 8, Gamache et al disclose a burn in tool (test fixture 8) for burning in at least one I/C chip (IC chip 12) comprising: a structure (socket 22) for mounting each chip (12) to be burned in; a power source (power source 44) to supply electrical current to burn in each chip; a structure (computer 48) for continuously monitoring at least one electrical value input to each chip (12) selected from the group of current, voltage and power, and a structure (combination of power source 44 and power sensor 46) to vary the voltage to maintain at least one of the values at or below a given value. However, Gamache et al do not disclose maintain the current value at

or below a given value. Iino et al disclose [see Fig. 6] controlling the burning in of at least one I/C chip (IC chip on wafer W) in a burn in tool (inspection section 12), wherein said tool (12) has a device (probe card 20) for mounting each chip (IC on wafer W) to be burned in, and a power source (power source 40) to supply electrical current to burn in each chip (IC on wafer W), comprising the steps of: continuously monitoring [via measuring section 41] at least one electrical value input to each chip (on wafer W) wherein the current value is maintain at or below a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13]. Further, Iino t al teach that the addition of maintaining current value at or below given value is advantageous because it prevents over current as well as to detect defects of the IC in a wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Gamache et al by adding a measuring section as taught by Iino in order to prevent over current as well as to detect defects of the IC in a wafer.

Regarding claim 9, Gamache et al disclose a burn in tool (test fixture 8) for burning in at least one I/C chip (IC chip 12) comprising: a structure (socket 22) for mounting each chip (12) to be burned in; a power source (power source 44) to supply electrical current to burn in each chip; a structure (computer 48) for continuously monitoring at least one electrical value input to each chip (12) selected from the group of current, voltage and power, and a structure (combination of power source 44 and power sensor 46) to vary the voltage to maintain at least one of the values at or below a given value. However, Gamache et al do not disclose maintain the current value at or below a given value. Iino et al disclose [see Fig. 6] controlling the burning in of at least one I/C chip (IC chip on wafer W) in a burn in tool (inspection section 12), wherein said tool (12) has a device (probe card 20) for mounting each chip (IC on wafer W) to be burned in, and a power

source (power source 40) to supply electrical current to burn in each chip (IC on wafer W), comprising the steps of: continuously monitoring [via measuring section 41] at least one electrical value input to each chip (on wafer W) wherein the power value is maintain at or below a given value [see col. 2, lines 9-30, col. 5, lines 3-63, col. 6, lines 29-37 and col. 7, line 47-col. 8, line 13]. Further, Iino t al teach that the addition of maintaining power value at or below given value is advantageous because it prevents over current as well as to detect defects of the IC in a wafer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Gamache et al by adding a measuring section as taught by Iino in order to prevent over current as well as to detect defects of the IC in a wafer.

***Conclusion***

5. Applicant's arguments with respect to claims 2-3 and 8-9 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on (517) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
September 19, 2005